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No k i h l I s l m

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The automotive industry has long been a leader in technological innovation, primarily
concerns with safety regulations. Exemption for ADAS, in particular, is a contentious issue, and a

Gold (Au) wire has been used in the automotive industry for many years, but due to its high cost and susceptibility to oxidation, it is being replaced by other materials. Palladium (Pd) wire is a common alternative to Au wire for electronic applications. There are various challenges associated with using such materials, including lower shear strength, but it is being used in automotive applications. Moving to qualify Cu wire for automotive applications is a goal.

Punched QFN or side solderable QFN with 10 pins is typically used in automotive applications. Roughened leads improve solderability (EMC) and where side solderable design is used, QFN packaging is preferred. The typical side solderable QFN is shown in Figure 2.

Figure 2: Typical side solderable QFN package

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Due to the increasing complexity of automotive applications, the packaging industry is moving towards high pin-count, fine-pitch packaging for automotive applications. High pin-count, fine-pitch packaging for automotive applications is a goal. High pin-count, fine-pitch packaging for automotive applications is a goal. High pin-count, fine-pitch packaging for automotive applications is a goal.

Silicon integration in the automotive industry is a goal. Silicon integration in the automotive industry is a goal. Silicon integration in the automotive industry is a goal.

Figure 3: Typical IC packages road map for repute into it oi nse dis hbor d

System level integration is il s or h p e v e n l i p a k g e s f i i g p u d r i e p a s d o w f s i m u l o u t e W L B S i P . T h e s t a n d a r d e f i n e d i n t e r f a c e s r e p l a c e s i n t e r f a c e s b e t w e e n r e d i s t r i b u t i o n l a y e r s t h a t i n h e r e n t l y r e m o v e d i n e d t a h o r e t c i r r a n d i n e b o s i g n i f i c a n t l y r e d u c e d i m p e d e n c e . A d v a n c e d F O W L P v i e s n o o l w h a t i n f o r t h i n h i g h e r l e v e l o f i n t e g r a t i o n p a k g e s s i . T h e i d e e s i n g g o e x p l i c i t l y o f t h i n t e g r a t i o n o f s u s i n e i s p , i n e d d i t d e s o p e n d e i n s t e r s e i t n e t o l m e p a k g e .

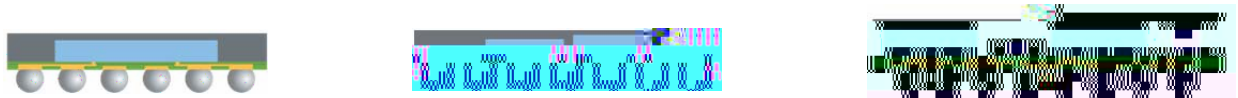


Figure 4: Multi Chip FOWLP (fan-out wafer level package)

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One of the basic requirements for the package is to be able to handle the high power and high frequency

Tbl e 2:Fn-o u t wif e d i g e D O E l f p r AEC-Q100 t e s t

Tbl e 3:Fn-o u t P d i g e i n d B o i r d L e v e l R e l i a b i l i t y T e s t R e s u l

5 H I H U H Q F H V

1. A u t o m o t i v e S e m i c o n d u c t o r s I n c . , 2 0 1 5 .
2. A l b e r t o S i n g i o v i n n i - V i n c e n t e l l i , “ A n d C h i p L e v e l E l e c t r o n i c s T o r f e A u d i t s E n g i n e e r s , I n c . 2 0 0 0
3. J i t o Y u , i n d B o g d a n M . W i l m o w s k i , “ R e c e n t A d v a n c e s i n S y s t e m s ” , I E E E , 2 0 1 1 , p p . 4 6 2 3 - 4 6 2 5
4. B i j i m s h i d i , “ A d v a n c e d W i f e r - L e v e l P d i g i n i g (W L P) E q u i l e n c y H A D A S R d i r s ” , C h i p S c l e R e v i e w , S e p - O c t , 2 0 1 6 , p p . 4 7 - 5 0 .
5. = P